LBL CCD Operating Procedures

CCD Voltages

Typical voltages for LBL CCDs are:

Signal	**Signal name**	**Typical Voltage**	**Notes**
Substrate Bias	Vsub	40V-80V	Optimum performance at highest voltage, possible breakdown at higher voltages. Use high impedance supply (>10 kohm). Use Vsub=0V during persistent image erase.
Output Drain	Vdd	-22V	Low gain below –20V, transistor glow, breakdown above –25V
Reset Drain	Vr	-13V	Sets the output working point. Use Vr and Vog to prevent charge injection. Normally 12.5V
Output Gate	Vog	5V	Prevents charge injection. Adjust in conjunction with Vr if necessary. If Vog is too high serial CTE is compromised. Normally 2.16 V
Vertical Clocks	V1,V2,V3, FS1,FS2,FS3	+5V -3V	Increase high side to +6V to erase persistent image. Typically connect FS1 to V1…to read out the entire CCD (no frame store)
Transfer Gate	Tg	+5V -3V	If parallel CTE is compromised try adjusting Tg first.
Horizontal Clocks	H1,H2,H3	+6V -4V	
Summing Well	SW	+5V -5V	

P+ guard is grounded, N+ guard is not connected, except during persistent image erase, when it is grounded.

The video output signal will be at about –18V if driving a 20 kOhm load.

CCD Pinout

V sub	1
H1 U	2
H2 U	3
H3 U	4
V r U	5
RG U	6
Video U	7
V dd U	8
V opg U	9
SW U	10
TG	11
p+ guard	12
FS1	13
FS2	14
FS3	15
V1	16
V2	17
V3	18
n+ guard	19
V sub	20

The LBL CCDs have two readout transistors. Each transistor and it's respective half of the serial register along with one copy of all parallel signals is brought out on 20 bond pads on one side of the chip (see table on left).

When looking at the connector side of the CCD with the connector on the left side the upper half of the CCD is referred to as the U-side, the lower half as the L-side.

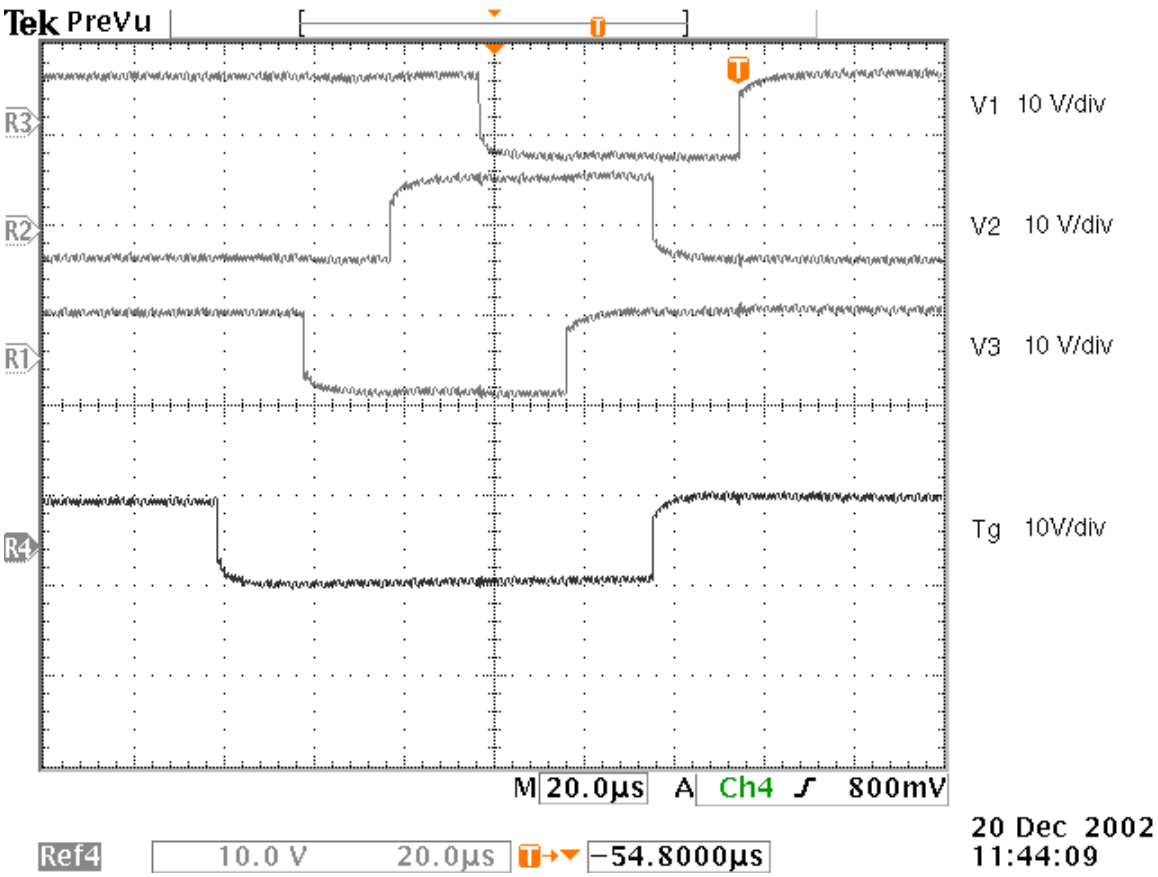
Connector Pinout:

Signal name	Nanonics pin
OG L	1
SW L	2
P+	3
P+	4
Nsub	5
N.C.	6
N.C.	7
N.C.	8
N+	9
V3	10
V2	11
V1	12
FS3	13
FS2	14
FS1	15
Nsub	16
TG	17
SW U	18
P+	19
OUT L	20
P+	21
VDD L	22
VR L	23
RG L	24
H3 L	25
H2 L	26
H1 L	27
H1 U	28
H2 U	29
H3 U	30
RG U	31
VR U	32
VDD U	33
P+	34
OUT U	35
P+	36
OG U	37

The Connector is a dual-row 37 pin Nanonics Dualobe (now owned by Tyco/Microdot) connector with metal body. It has holes for M1 jack-screws (newer versions will have the more robust M1.2.)
The connector is a vertical mount socket.

When connecting or disconnecting the Nanonics Connector great care must be taken to move it parallel. The jack screws should be turned alternating not more than one turn at a time.

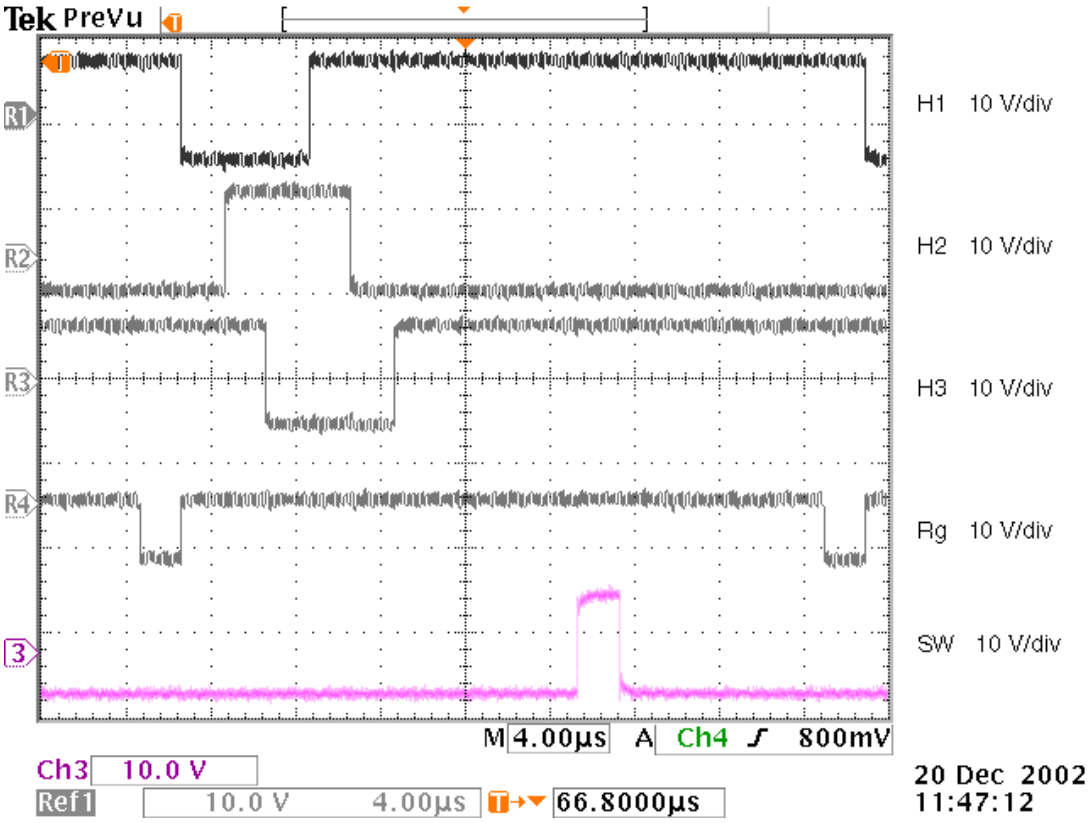
Typical Waveforms



Parallel waveforms for slow clocking with 20 us overlap. Overlap can be reduced below 10 us to increase readout speed if wiring between drivers and CCD is short enough.

The current 2kx4k CCD has 2048 +12 dummy serial pixels and 4096 parallel pixels.

During integration phases 1 and 2 should be low.



Serial clock waveforms for 30 kHz readout to the L transistor.
Note that H1 and H3 are symmetrical around H2, so swapping of H1 and H2 reverses the clocking direction in the serial register, enabling readout to the U transistor.
If the horizontals on the L side are clocked with the above pattern, while on the U side H1 and H3 are reversed the CCD is read out to both transistors simultaneously.

Reduction of the clock overlap, settling and integration times can increase readout speed to 100 kHz with modest noise gains.
The serial clock overlap as well as the reset low time can be reduced to 160 ns.
The summing well high time can be reduced to 500 ns.
The integration time can be reduced to 3760 ns (or below with increased read noise).
The settling time (between the last clock transition and the begin of integration) can be reduced to 120 ns.

These minimum values worked well in our system, but may not be optimal for your setup due to different cabling length, preamp input capacitance, and other parasitic capacitances.
Note however that the SDSU Gen II controller has problems at 100 kHz in the slow integration speed setting due to excessive impedance in the integration capacitor reset circuitry. The high-speed setting does not have those problems, but the higher gain in this setting will saturate the ADC below full well level.
See SDSU controller modification pages for options.

Persistent Image Erase

To erase persistent images, and to achieve ultimate dark current after initial power-up the CCD should be erased. Different procedures have been successfully used.
One option is to reduce the Substrate bias below 30V, then short N+ to ground, while driving the parallel clocks at +6V high level. It is important that the impedance of the substrate bias power supply is large enough to prevent a current of more than a few mA from flowing between Vsub and N+. If in doubt further reduce Vsub during the erase.

The second option does not require wiring of the N+ guard. During erase the substrate bias is clamped to ground while the parallel clocks are driven to +6V. This simpler procedure has been reported to work well, but we do not have extensive experience with the achievable level of dark current.
The ramp-up of the substrate voltage has to be done in a controlled fashion to prevent excessive charge injection which can over-saturate the CCD.